AMENDMENT TO THE CLAIMS

This Listing of Claims will replace all prior versions, listing, of claims in the specification.

LISTING OF CLAIMS:

Claim 1 (original) An ESD protection circuit applied to an IC with power-down-mode operation, comprising:

an input circuit, which comprises:

an input pad;

an input PMOS, wherein the drain of said input PMOS is connected to said input pad;

an input NMOS, wherein the drain of said input NMOS is connected to said input pad; and

a first internal circuit connected to said input pad through at least one resistor;

an output circuit, which comprises:

an output pad;

an output PMOS, wherein the drain of said output PMOS is connected to said output pad;

an output NMOS, wherein the drain of said output NMOS

is connected to said output pad; and

a second internal circuit connected to the gate of said PMOS and the gate of said NMOS;

a VDD power line connected and providing VDD voltage to said first internal circuit and said second internal circuits;

a VSS power line connected and providing VSS voltage to said first internal circuit and said second internal circuits, said VSS power line still connected to the source and the gate of said input NMOS and the source of said output NMOS;

an ESD bus line connected to the source and the gate of said input PMOS;

a first ESD clamp circuit connected between said VSS power line and said ESD bus line;

a second clamp circuit connected between said VDD power line and said VSS power line;

a first diode forward connected between said VDD power line and said ESD bus line to avoid leakage current induced from said input pad to said VDD power line, and to avoid positive voltage at said input pad charging to said VDD power line through said input PMOS;

a second diode forward connected between said VDD power line and the source of said output PMOS to avoid leakage current induced from

said output pad to said VDD power line, and to avoid positive voltage at said output pad charging to said VDD power line through said output PMOS; and

a third diode, wherein the negative terminal of said third diode is connected to said ESD bus line and the coupled node connected to the positive terminal of said third diode is selected from said output pad and the source of said output PMOS.

Claim 2 (original) The ESD protection circuit of claim 1, wherein the positive terminal of said third diode is connected to the output pad and then positive charge at said input pad discharges to said VSS power line through said input PMOS, said ESD bus line, and said first ESD clamp circuit under positive-to-VSS ESD mode, and furthermore the positive charge at said output pad discharges to said VSS power line through said third diode, said ESD bus line, and said first ESD clamp circuit under positive-to-VSS ESD mode.

Claim 3 (original) The ESD protection circuit of claim 1, wherein the positive terminal of said third diode is connected to the source of said output PMOS and then positive charge at said input pad discharges to said VSS power line through said input PMOS, said ESD bus line, and said first ESD clamp circuit under positive-to-VSS ESD mode, and furthermore the positive charge at said output pad discharges to said VSS power line through said output PMOS, said third diode, said ESD bus line, and said first ESD clamp circuit under positive-to-VSS ESD mode.

Claim 4 (original) The ESD protection circuit of claim 1, wherein the positive terminal of said third diode is connected to the output pad and then positive charge at said input pad discharges to said VDD power line through said input PMOS, said ESD bus line, said first ESD clamp circuit, said VSS power line, and said second ESD clamp circuit under positive-to-VDD ESD mode, and furthermore the positive charge at said output pad discharges to said VDD power line through said third diode, said ESD bus line, said first ESD clamp circuit, said VSS power line, and said second clamp circuit under positive-to-VDD ESD mode.

Claim 5 (original) The ESD protection circuit of claim 1, wherein the positive terminal of said third diode is connected to the source of said output PMOS and then positive charge at said input pad discharges to said VDD power

line through said input PMOS, said ESD bus line, said first ESD clamp circuit, said VSS power line, and said second ESD clamp circuit under positive-to-VDD ESD mode, and furthermore the positive charge at said output pad discharges to said VDD power line through said output PMOS, said third diode, said ESD bus line, said first ESD clamp circuit, said VSS power line, and said second clamp circuit under positive-to-VDD ESD mode.

Claim 6 (original) The ESD protection circuit of claim 1, wherein negative charge at said input/output pad discharges to said VSS power line through said input/output NMOS under negative-to-VSS ESD mode.

Claim 7 (original) The ESD protection circuit of claim 1, wherein negative charge at said input/output pad discharges to said VDD power line through said input/output NMOS, said VSS power line, and said second ESD clamp circuit under negative-to-VDD ESD mode.

Claim 8 (original) The ESD protection circuit of claim 1, which can construct repeatedly to form a multi-stage ESD protection circuit, wherein the output pad of the previous stage of said ESD protection circuits is connected to the input pad of the next stage of said ESD protection circuit.

Claim 9 (original) The ESD protection circuit of claim 1 further comprising at least one output swing improvement circuit connected between said VDD power line and the source of said output PMOS for compensating the voltage drop induced by said second diode.

Claim 10 (original) The ESD protection circuit of claim 9, wherein said output swing improvement circuit comprises:

a NMOS, wherein the gate and the source of said NMOS are connected to said VDD power line and said VSS power line, respectively;

a first PMOS, wherein the source, the gate and the drain are connected to said VDD power line, the drain of said NMOS, and the source of said output PMOS, respectively; and

a second PMOS, wherein the source, the gate and the drain are separately connected to the gate of said first PMOS, said VDD power line, and the source of said output PMOS, and then said second PMOS turning off and said NMOS turning on when said VDD voltage is high and thus said VDD voltage coupling to said output PMOS via said first PMOS instead of through said second diode so as to avoid voltage drop induced by said second diode.

Claims 11-12 (canceled).

Claim 13 (original) The ESD protection circuit of claim 11 further comprising at least one output swing improvement circuit connected between said VDD power line and the source of said output PMOS for compensating voltage drop induced by said second diode.

Claim 14 (original) An ESD protection circuit applied to an IC with power-down-mode operation, comprising:

an input pad;

an input PMOS, wherein the drain of said input PMOS is connected to said input pad;

an input NMOS, wherein the drain of said input NMOS is connected to said input pad; and

an internal circuit connected to said input pad through at least one resistor;

an output PMOS, wherein the gate of said output PMOS is connected to said internal circuit;

an output NMOS, wherein the gate of said output NMOS is connected to said internal circuit;

an output pad connected with the drain of said PMOS and the drain of said NMOS;

a VDD power line connected and providing VDD voltage to said internal circuit;

a VSS power line connected and providing VSS voltage to said internal circuit and still connected to the source and the gate of said input NMOS and the source of said output NMOS;

an ESD bus line connected to the source and the gate of said input PMOS;

a first ESD clamp circuit connected between said VSS power line and said ESD bus line;

a second clamp circuit connected between said VDD power line and said VSS power line;

a first diode forward connected between said VDD power line and said ESD bus line to avoid leakage current induced from said input pad to said VDD power line which is grounded under power-down-mode operation, and still to avoid positive voltage at said input pad charging to said VDD power line via said input PMOS when said VDD power line is floating under power-down-mode operation;

a second diode forward connected between said VDD power line and the source of said output PMOS to avoid leakage current induced from said output pad to said VDD power line via said output PMOS when said VDD power line is grounded under power-down-mode operation, and still

to avoid positive voltage at said output pad charging to said VDD power line through said output PMOS when said VDD power line is floating under power-down-mode operation; and

a third diode, wherein the negative terminal of said third diode is connected to said ESD bus line and the coupled node connected to the positive terminal of said third diode is selected from said output pad and the source of said output PMOS.

Claim 15 (original) The ESD protection circuit of claim 14, which can construct repeatedly to form a multi-stage ESD protection circuits, wherein the output pad of the previous stage of said ESD protection circuit is connected to the input pad of the next stage of said ESD protection circuit.

Claim 16 (original) The ESD protection circuit of claim 14 further comprising at least one output swing improvement circuit connected between said VDD power line and the source of said output PMOS for compensating the voltage drop induced by said second diode.

Claims 17-18 (canceled).

Claim 19 (original) The ESD protection circuit of claim 17 further comprising at least one output swing improvement circuit connected between said VDD power line and the source of said output PMOS for compensating voltage drop induced by said second diode.

Claim 20 (original) The ESD protection circuit of claim 19, wherein said output swing improvement circuit comprises:

a NMOS, wherein the gate and the source of said NMOS are connected to said VDD power line and said VSS power line, respectively;

a first PMOS, wherein the source, the gate and the drain are connected to said VDD power line, the drain of said NMOS, and the source of said output PMOS, respectively; and

a second PMOS, wherein the source, the gate and the drain are separately connected to the gate of said first PMOS, said VDD power line, and the source of said output PMOS, and then said second PMOS turning off and said NMOS turning on when said VDD voltage is high and thus said VDD voltage coupling to said output PMOS via said first PMOS instead of through said second diode so as to avoid voltage drop induced by said second diode.